REMARKS

The claims are claims 1 to 9.

Claims 1 and 5 were amended. Claims 8 and 9 are added. Claims 1 and 5 are amended to further distinguish over the cited references. Claims 8 and 9 recite subject matter not previously claimed disclosed in the application at page 5, line 20 to page 6, line 21.

Claims 1, 2 and 4 to 6 were rejected under 35 U.S.C. 102(b) as anticipated by Maki et al, European Published Application 0 536 414 A1.

Claims 1 and 5 recite subject matter not anticipated by Maki et al. Claim 1 recites "storing image data in a memory having data words of a predetermined data width, each data word including said first predetermined number of image pixels adjacently disposed on a single scan line, a set of said second predetermined number of consecutive data words corresponding to a two dimensional tile of an image." Claim 5 similarly recites "a memory storing image data having data words of a predetermined data width, each data word including a first predetermined number of image pixels adjacently disposed on a single scan line, a set of a second predetermined number of consecutive data words corresponding to a two dimensional tile of said first predetermined number of image pixels and said second predetermined number of scan lines of an image." This manner of storing the image data in memory is not anticipated by Maki et al. Maki et al states at column 6, lines 40 to 49 (cited in the rejection):

> "Fig. 6 shows the arrangement of image data in the image data memory 52. This figure exemplifies an image data memory 52 which can store therein and image data having 2048 dots in row and 1024 dots in column. That is, supposing that 1 dot corresponds to 1 bit and 1 word corresponds to 32 bits, the image data memory 52 can store therein image data having the

capacity of 65536 words. Denoted at 201 is a word and numerals in words represent word numbers respectively."

Maki et al further states at column 7, lines 6 to 8:

> "Denoted at 202 in Fig. 6 is a memory area having the capacity equal to that of the cache memory 102 for storing data therein."

This disclosure of Maki et al is contrary to the above quoted limitation of claims 1 and 5. Assuming that memory area 202 corresponds to the claimed two dimensional tile, words 201 of Maki et al are not disposed as claimed. Figure 6 of Maki et al clearly illustrates that each row of memory area 202 includes plural words 201. To the contrary, claims 1 and 5 recite that each data word includes the "first predetermined number of image pixels" of that scan line of the tile. Since claims 1 and 5 recite a single data word per scan line of the tile and Maki et al discloses plural data words 201 per scan line of area 202, claims 1 and 5 are not anticipated by Maki et al.

Claims 1 and 5 recite further subject matter not anticipated by Maki et al. Claims 1 and 5 each recite "whereby adjacent data words include image pixels of adjacent scan lines." Figure 6 of Maki et al illustrates several pairs of adjacent words 201: 0 and 1; 62 and 63; 64 and 65; 65440 and 65441; 65470 and 65471; 65472 and 65473; and 65534 and 65535. Figure 6 clearly illustrates that each of these adjacent words 201 are disposed on the same scan line and the claimed adjacent scan lines. Accordingly, claims 1 and 5 are not anticipated by Maki et al.

Claims 2, 4 and 6 are allowable by dependence upon allowable claims 1 and 5.

Claims 3 and 7 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Maki et al and Mita et al, U.S. Patent No. 5,293,481.

Claims 3 and 7 recite subject matter not made obvious by the combination of Maki et al and Mita et al. Claim 3 recites "said steps of transferring a tile of image data from the memory into the cache, performing image operations upon said tile of image data transferred to the cache, and transferring said tile of image data from the cache to the memory are performed by different data processors for different tiles." Claim 7 recites a second data processing apparatus and "wherein said data processing apparatus and said second data processing apparatus are programmed to operate upon different tiles of image data simultaneously." Mita et al states at column 33, lines 51 to 64 (cited in the rejection):

> "FIG. 57 is a view showing the relationship among an input pixel block 591 corresponding to an original image 590, pixels 591a, a processor unit 592, processor elements 592a, and output image data 593a in an output image memory 593. In accordance with a control signal from a controller 594, the image data block 591 of 16 pertinent pixel elements in the original image memory 590 on the input side are accessed simultaneously, and the image data are accepted by respective ones of the processor elements 592a in the processor unit 562. The processor unit 592 computes typical density information 571 and detail information 572 such as shown in FIG. 55 from the 16 pixels of image data 591, and outputs the results to the image memory 593 on the output side."

This portion of Mita et al makes clear that pixel block 591 consists of pixels 591a. When pixel block 591 is accessed by processor unit 592, individual pixels 591a are processed by processor elements 592a. Thus a single tile (pixel block 591) is processed by a single processor (processor unit 592). Mita et al states at column 34, lines 45 to 60 (cited in the rejection):

> "By repeating the above-described processing through sequentially accessing the original image memory on the input side in 4.times.4 pixels block units until the compression processing for the final 4.times.4 pixels block of the

original image memory is concluded, compression data equivalent to one page of the original image can be obtained.

"In accordance with the present embodiment as described above, the raw data of the inputted original image, is sequentially accessed every memory block of mXn pixels (e.g. 44 pixels). Therefore, rather than accessing each pixel in the image memory on the input side a plurality of times, mXn pixels of image data can be accessed simultaneously. This makes it possible to transfer the image data while it is being compressed at high speed. "

This portion of Mita et al clearly teaches repeated use of a single processing unit 592 to sequentially process pixel blocks 591 of the image 590. This fails to teach the use of plural processors to process plural tiles as recited in claims 3 and 7. Accordingly, claims 3 and 7 are not made obvious by the combination of Maki et al and Mita et al.

Claims 8 and 9 recite subject matter not anticipated by nor made obvious by Maki et al and Mita et al. These references fail to teach that a tile access includes the second predetermined number of page mode accesses. Accordingly, claims 8 and 9 are allowable.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, the Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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